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| EXAMINER | |
|---|---|
| FAHERTY, COREY S | |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2183 | |

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**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

ip.department.us@nxp.com

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/583,052 | DYTRYCH, PETER | |
| | Examiner | Art Unit | |
| | Corey S. Faherty | 2183 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *23 June 2009*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-3,6-10 and 12-17* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3,6-10 and 12-17* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

## DETAILED ACTION

1. This office action is in response to the reply filed on 06/23/2009.

2. Claims 1-3, 6-10 and 12-17 are pending in the application and have been examined.

### *Claim Rejections - 35 USC § 103*

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

5. Claims 1-3, 6-7, 10 and 12-17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Suzuki (EP 1 046 983) in view of Faraboschi et al. (U.S. Patent 5,930,508), referenced from here forward as Faraboschi.

6. Regarding claims 1, 12 and 15, Suzuki discloses a parallel processing apparatus for processing data based on instruction words comprising at least two individual instructions used for controlling at least two respective functional units, [page 6, paragraph 0039; a processor

contains at least two processing units, each of which processes an instruction of a very long instruction word], said apparatus comprising:

an instruction processor arranged to process a first individual instruction extracted from a first instruction word, and at least a second individual instruction extracted from at least a subsequent second instruction word, as a new single instruction word [pages 6-7; paragraphs 0043-0048; instructions are compressed by combining individual instructions from multiple instruction words]; and

a program memory arranged to store said single instruction word [page 8, paragraph 0061; the compressed instruction is stored in a memory].

Suzuki does not explicitly disclose that the processor is further arranged to add a predetermined control information to said single instruction word, said control information indicating an allocation of said extracted first and at least second individual instructions to said respective functional units and a sequential order of said first and least second individual instructions at their respective functional units.

However, Faraboschi discloses an instruction compression technique similar to that of Suzuki in which nops are removed from the original instruction words and the remaining instructions are combined [col. 2, line 66 – col. 3, line 15]. In the system of Faraboschi, the processing means is arranged to add a predetermined control information to the compressed instruction word [col. 4, line 57 – col. 5, line 35], said control information indicating at least one of an allocation of said extracted first and at least second individual instructions to said respective functional units [col. 4, lines 65-66] and a sequential order of said first and least second individual instructions at their respective functional units [col. 5, lines 12-39].

It would have been obvious to use the compression techniques of Faraboschi in the compression system of Suzuki because doing so allows for more efficient compression and execution of the instructions due to increased opportunity for compression.

7. Regarding claim 2, Suzuki in view of Faraboschi discloses an apparatus according to claim 1, wherein said instruction processing means is arranged to extract said first and at least second individual instructions if said first and at least second instruction words each comprise one of predetermined instruction patterns with at least one delay instruction, and to compress said first and at least second instruction words into said single instruction word [Suzuki, pages 6-7; paragraphs 0043-0048; instructions are compressed when nops exist].

8. Regarding claim 3, Suzuki in view of Faraboschi discloses an apparatus according to claim 2, wherein said delay instruction is a null operation [Suzuki, pages 6-7; paragraphs 0043-0048; instructions are compressed when nops exist].

9. Regarding claims 6 and 16, Suzuki in view of Faraboschi discloses an apparatus according to claim 1, wherein said control information consists of at least one bit added as at least one respective most significant bit to said single instruction word [Faraboschi, col. 5, lines 13-35].

10. Regarding claim 7, Suzuki in view of Faraboschi discloses an apparatus according to claim 1, wherein said instruction processing means is arranged to check said control information in an instruction word read from a program memory to re-establish said first and at least instruction words based on said control information, and to supply said re-established first and at least second instruction words to an instruction decoder [Faraboschi, col. 5, lines 13-18].

11. Regarding claim 10, Suzuki in view of Faraboschi discloses an apparatus according to claim 1, wherein said parallel processing apparatus is a VLIW processor [Suzuki, title].

12. Regarding claim 13, Suzuki in view of Faraboschi discloses a computer program product comprising code means for controlling a computer system so as to perform the steps of a compression method according to claim 12 when loaded into said computer system [Suzuki, page 8, paragraph 0061].

13. Regarding claim 14, Suzuki in view of Faraboschi discloses an apparatus according to claim 1, wherein said new single instruction word further includes a third individual instruction extracted from a subsequent third instruction word [Faraboschi, Figures 4,5; a compacted instruction word may include three or more instruction syllables].

14. Regarding claim 17, Suzuki in view of Faraboschi discloses a method according to claim 12, further comprising: reading the stored single instruction word [Faraboschi, col. 5, lines 36-39; the compacted instruction is read]; checking said control information in the read single instruction word [Faraboschi, col. 5, lines 36-39; the delimiter bits are used]; re-establishing said first and at least second instruction words based on said control information [Faraboschi, col. 5, lines 36-39; the delimiter bits are used to differentiate the original instructions]; and decoding said re-established first and at least second instruction words [Faraboschi, Fig. 6; col. 5, lines 46-60; instructions are dispersed to be executed].

15. Claims 8-9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Suzuki in view of Faraboschi as applied to claim 1 above, and further in view of Iwata et al. (U.S. Patent 6,275,921), referenced from here forward as Iwata, and Topham (U.S. Patent Application Publication 2001/0047466).

16. Regarding claim 8, Suzuki in view of Faraboschi does not explicitly disclose that all instruction words associated with delay slots and branch targets are marked, wherein extraction of instruction words is based on the markings. However, Suzuki analyzes all instruction types to determine which will be extracted and therefore, in a system having delay slots and branch instructions, it would be obvious to mark those specific types of instructions in order to analyze them for potential extraction. Furthermore, as is well-known in the art, as well as being taught by Iwata [col. 19, lines 15-63] and Topham [page 6, paragraphs 0075-0077], delay slot instructions and target instructions must be executed with their specific basic block and therefore care must be taken when compressing such instructions with other instructions. It therefore would have been obvious to a person having skill in the art to mark these types of instructions and base any compression or extraction of instructions on those markings.

17. Regarding claim 9, Suzuki in view of Faraboschi, Iwata and Topham discloses an apparatus according to claim 8, wherein said instruction processing means is arranged to adjust at least one program memory address based on a decided extraction [Topham, page 1, paragraph 0011].

### *Response to Arguments*

18. Applicant's arguments filed 06/23/2009 have been fully considered but they are not persuasive.

19. Applicant first argues that the proposed combination of Suzuki and Faraboschi would undermine the stated purpose of the Suzuki reference to provide compression without assigning special bits to an instruction field and that there is therefore no reason for one having skill in the

art to form the combination. The examiner respectfully disagrees. A person having skill in the art will recognize the benefits of adding the techniques of Faraboschi to Suzuki. The addition of control bits such as taught by Faraboschi allows for more instructions to be compressed because those instructions do not need to meet the same criteria that instructions in the system of Suzuki must meet in order to be compressed. Furthermore, the use of the delimiter encoding bits in Faraboschi allows, for instance, for a compacted instruction word to be stored across address boundaries [col. 6, lines 3-6], resulting in more efficient compression of those instructions. The use of dispersal bits also allows the compacted instructions to be quickly and easily forwarded to the appropriate functional unit without needing to decode the instruction. For at least these reasons, the addition of the techniques of Faraboschi to Suzuki would be obvious to a person having skill in the art.

Applicant has argued that a person having skill in the art would not combine the two references because the techniques of Faraboschi allegedly undermine Suzuki's purpose. The examiner respectfully disagrees. The teachings of Faraboschi do not undermine the teachings of Suzuki. Faraboschi simply offers another design option and discusses the benefits of using that option (as outlined in the previous paragraph). Applicant's attempt to portray a difference in design choice as an undermining of Suzuki's purpose is not persuasive because it is common that different design options result in different benefits. Faraboschi has given clear examples of the benefits of his technique and a person having skill in the art will use that technique when those benefits suit the needs of the system.

Applicant has further argued, in response to the above arguments, that even though Faraboschi provides clear motivation for using additional bits, the combination is not proper

because Suzuki has disclosed the concept of not using additional bits. Applicant continues to repeat this argument without ever actually addressing the examiner's position. Applicant's argument relies on the assumption that one of the techniques is always superior to the other and that a person having skill in the art could not recognize that both techniques have potential benefits. However, this is rarely the case in the design of a processing system. Specifically, while Suzuki discloses the method of not using additional bits, Suzuki does not say that this is always the best method to use. On the contrary, Suzuki simply offers potential benefits of using this method. Similarly, Faraboschi discloses possible benefits of using additional bits. It is the job of a system designer to analyze the benefits of each method and determine the best fit for the system that is being designed. For instance, a system that has a limited hardware budget would likely be better off not using additional bits and thus avoiding the additional hardware of Faraboschi. On the other hand, a system that has a surplus of hardware budget but requires fast and efficient forwarding of instructions would likely welcome the additional hardware disclosed by Faraboschi. The examiner's position is that, in such a situation, a person having skill in the art would correctly apply the teachings of Faraboschi to the system of Suzuki.

It should also be noted that the execution of compressed instructions without the use of additional bits is merely one of many stated objectives of the Suzuki reference. Numerous embodiments disclosed by Suzuki (including those referenced by the examiner in the rejections) do not even reference the lack of additional bits. As can be seen from paragraphs [0017] to [0031], the primary objective is for efficient processing of VLIW instructions, an objective that is helped by the addition of Faraboschi.

20. Applicant next argues that the delimiter bits of Faraboschi do not indicate a sequential order of instructions. The examiner respectfully disagrees. The delimiter bits are used to indicate the point at which one instruction ends and the next begins. Without the delimiter bits, it would be impossible to determine a sequence because there would be no indication that a next instruction had started. Applicant's argument is therefore not persuasive.

Applicant has made no argument in response to the above position, other than to simply make conclusory statements. As explained above, the examiner's position is that, if you have a block of data without delimiter bits, you don't know where one instruction ends and where the next begins. If you don't know where one instruction ends and where the next begins, you don't know the sequential order of instructions (because you don't even know where the instructions are). The delimiter bits are used to determine where the instructions begin and end, and thus are used to determine a sequential order. Applicant's argument apparently relies on a more specific interpretation of the claim phrase. If such a specific interpretation is critical to the invention, the examiner respectfully suggests that it be explicitly recited in the claim.

Furthermore, Faraboschi explicitly discloses that the delimiter bits are utilized by the instruction sequencer to determine the sequence of incoming instructions [col. 5, lines 36-45]. Applicant has not addressed these teachings in the arguments presented.

## *Conclusion*

21. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Corey S. Faherty whose telephone number is (571) 270-1319. The examiner can normally be reached on Monday-Thursday and every other Friday, 7:00-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Eddie P Chan/
Supervisory Patent Examiner, Art Unit 2183

/Corey S Faherty/
Examiner, Art Unit 2183